SYSTEM AND METHOD FOR BALANCING CAPACITIVELY COUPLED SIGNAL LINES

ABSTRACT OF THE DISCLOSURE

A signal balancing circuit for capacitively coupled signaling between transmitting and receiving devices over a plurality of capacitively coupled signal lines on which data signals are transmitted from the transmitting device to the receiving device. The signal balancing circuit includes an encode circuit for forcing a signal transition of a data signal for a data interval in response to the data signal maintaining the same logic state throughout a respective time interval. A balancing signal is generated having a logic level and a timing relative to the time intervals of the respective data signals indicative of inversion of a particular data signal. A decode circuit coupled to the encode circuit to receive the balancing signal forces a transition of the transitioned signal at the appropriate time in accordance with the balance signal to recover the original logic level of the data signal.